KALASALINGAM
ACADEMY OF RESEARCH AND EDUCATION
(DEEMED TO BE UNIVERSITY)
Under sec. 3 of UGC Act 1956.
Anand Nagar, Krishnankoil - 626126. Srivilliputtur (Via), Virudhunagar (Dt), Tamil Nadu | info@kalasalingam.ac.in | www.kalasalingam.ac.in
SCHOOL OF ELECTRONICS AND ELECTRICAL TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MASTER OF TECHNOLOGY
VLSI DESIGN

CURRICULUM AND SYLLABUS
(CBCS)

(For the Students Admitted from the Academic Year 2018-19 Onwards)


KALASALINGAM
ACADEMY OF RESEARCH AND EDUCATION
அறிவு
அற்றம் காக்கும்
கருவி

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SCHOOL OF ELECTRONICS AND ELECTRICAL TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

UNIVERSITY VISION

To be a Centre of Excellence of International Repute in Education and Research

UNIVERSITY MISSION

To Produce Technically Competent, Socially Committed Technocrats and Administrators through Quality Education and Research

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SCHOOL OF ELECTRONICS AND ELECTRICAL TECHNOLOGY
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT VISION

To become an internationally leading centre of higher learning and research in the domain of Electronics and Communication Engineering

MISSION

- *To provide quality education in the domain of Electronics and Communication Engineering through periodically updated curriculum, effective teaching learning process, best of breed laboratory facilities and collaborative ventures with the industries*
- *To inculcate innovative skills, research aptitude, team-work, ethical practices among students so as to meet expectations of the industry as well as society*

M.TECH. VLSI DESIGN PROGRAMME EDUCATIONAL OBJECTIVES

Within a few years of obtaining apostgraduate degree in Electronics and Communication Engineering with a specialisation of VLSI Design, the students will be able to:

PEO1: Have an in-depth knowledge along with new technical ideas, to analyse and evaluate the potential engineering problems and to contribute to the research and development in the core areas by using modern engineering and IT tools

PEO2: Demonstrate self – management and teamwork in a collaborative and multidisciplinary arena

PEO3: Have good professional practices with a responsibility to contribute to sustainable development of society

PEO4: Have a zeal for improving technical competency by continuous and corrective learning:

M.TECH. VLSI DESIGN PROGRAMME SPECIFIC OUTCOMES (R2018)

PSO1: Design and develop VLSI circuits to optimise power and area requirements, free from faults and dependencies by modelling, simulation and testing.

PSO2: Develop VLSI systems by learning advanced algorithms, architectures and software – hardware co – design.

PSO3: Communicate engineering concepts effectively by exhibiting high standards of technical presentations and scientific documentations

M.TECH. VLSI DESIGN PROGRAMME OUTCOMES (R2018)

At the end of the programme, the students will be able to:

Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialisation to the solution of complex engineering problems.

Problem analysis: Identify, formulate, research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions

Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal, and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

Individual and teamwork: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

Life-long learning: Recognise the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

M.TECH. VLSI DESIGN CURRICULUM

Curriculum Structure (As Per AICTE Model Curriculum 2018):

Sl.	Category	Credits
I.	Core Courses (Theory)	**15**
II.	Core Courses (Laboratory)	**8**
III.	Supportive Courses (Mathematics and Research Methodology)	**4**
IV.	Programme Specific Elective Courses	**15**
V.	Open Elective Courses (Interdisciplinary / General Elective)	**3**
VI.	Mini Project	**2**
VII.	Project Work	**26**
VIII.	Audit Courses (2 Courses)	**--**
	Total Credits	**73**

SCHEME OF INSTRUCTION

I. Core Courses (Theory)

S.	Course Code	Course Name	Type	Pre	L	T	P	Credits
1.	ECE18R5101	RTL Simulation and Synthesis with PLDs	T		3	0	0	3
2.	ECE18R5102	Designing with ASICs	T		3	0	0	3
3.	ECE18R5103	Analog and Digital CMOS VLSI Design	T		3	0	0	3
4.	ECE18R5104	VLSI Design Verification and Testing	T		3	0	0	3
5.	ECE18R6101	Microcontrollers and Programmable Digital Signal Processors	T		3	0	0	3
							Total	**15**

II. Core Courses (Laboratory)

S.	Course Code	Course Name	Type	Co-Requisite	L	T	P	Credits
1.	ECE18R5180	RTL Simulation and Synthesis with PLDs Laboratory	L	ECE18R5101	0	0	3	2
2.	ECE18R5181	ASIC CAD Laboratory	L	ECE18R5102	0	0	3	2
3.	ECE18R5182	Analog and Digital CMOS VLSI Design Laboratory	L	ECE18R5103	0	0	3	2
4.	ECE18R5183	VLSI Design Verification and Testing Laboratory	L	ECE18R5104	0	0	3	2

S.	Course Code	Course Name	Type	Co-Requisite	L	T	P	Credits
							Total	8

III. Supportive Courses

S.	Course Code	Course Name	Type	L	T	P	Credits
1.	MAT18R5001	Applied Mathematics	T	3	0	0	3
2.	PGM18R5001	Research Methodology for Engineers	T	0	1	0	1
						Total	4

IV. Programme Specific Elective Courses

Sl.	Course Code	Course Name	Type	Pre-requisite	L	T	P	C
1.	ECE18R5120	Network Security and Cryptography	T		3	0	0	3
2.	ECE18R5121	Semiconductor Device Modelling	T		3	0	0	3
3.	ECE18R5122	Scripting Languages for VLSI Design Automation	T	ECE18R5135	3	0	0	3
4.	ECE18R5123	VLSI Signal Processing	T		3	0	0	3
5.	ECE18R5124	Parallel Processing	T		3	0	0	3
6.	ECE18R5125	Submicron Technology	T	ECE18R5131	3	0	0	3
7.	ECE18R5126	VLSI Interconnects and its Design Techniques	T	ECE18R5135	3	0	0	3
8.	ECE18R5127	CAD of Digital System	T	ECE18R5135	3	0	0	3
9.	ECE18R5128	Programming Languages for Embedded Software	T		3	0	0	3
10.	ECE18R5129	Memory Technologies and Testing	T	ECE18R5104	3	0	0	3
11.	ECE18R5130	SoC Design	T		3	0	0	3
12.	ECE18R5131	Low Power VLSI Design	T	ECE18R5103	3	0	0	3
13.	ECE18R5132	Communication Buses and Interfaces	T		3	0	0	3
14.	ECE18R6120	Hardware Software Co-Design	T		3	0	0	3
15.	ECE18R5135	Physical Design Automation	T	ECE18R5102	3	0	0	3
16.	ECE18R6121	Three-Dimensional Network-On-Chip	T		3	0	0	3
17.	ECE18R6122	Quantum Electronics	T		3	0	0	3
18.	ECE18R6123	Nanomaterials and Nanotechnology	T		3	0	0	3

V. Open Elective Courses

Generic Electives Offered to VLSI Design students by Other Departments

Sl.	Course Code	Course Name	Type	L	T	P	C
1.	CSE18R5051	Cloud Computing	T	3	0	0	3
2.	CSE18R5052	IoT and Applications	T	3	0	0	3
3.	CSE18R5053	Big Data Analytics	T	3	0	0	3
4.	EEE18R5020	Soft Computing Techniques	T	3	0	0	3
5.	EEE18R5021	Optimization Techniques	T	3	0	0	3
6.	EEE18R6013	Evolutionary Computation Techniques	T	3	0	0	3

Interdisciplinary Electives Offered to VLSI Design students by Other Departments

Sl.	Course Code	Course Name	Type	L	T	P	C
1.	EEE18R5113	Renewable Power Generation	T	3	0	0	3
2.	MEC18R5151	Industrial Robotics and Expert Systems	T	3	0	0	3
3.	MEC18R5152	Avionics	T	3	0	0	3
4.	MEC18R5153	Mechatronics	T	3	0	0	3
5.	AUT18R5026	Automotive Electronics	T	3	0	0	3
6.	ICE18R5009	Robotics and Automation	T	3	0	0	3
7.	INT18R6023	Deep Learning Techniques	T	3	0	0	3
8.	INT18R6024	Operating Systems	T	3	0	0	3
9.	ICE18R6011	Smart Materials and Systems	T	3	0	0	3

VI. Mini Project (2 Credits)

S.	Course Code	Course Name	Type	L	T	P	Credits
1.	ECE18R5199	Mini Project	P	0	0	3	2
						Total	**2**

VII. Project Work (26 Credits)

S.	Course Code	Course Name	Type	L	T	P	Credits
1.	ECE18R6198	Project Work PhaseI	P	0	0	20	10
2.	ECE18R6199	Project Work Phase II	P	0	0	32	16
						Total	**26**

VIII. Audit Courses (2 Courses)

Sl.	Course Code	Course Name	Type	L	T	P	C
1.	AUD18R5001	English for Research Paper Writing	T	2	0	0	0
2.	AUD18R5002	Pedagogy Studies	T	2	0	0	0

Interdisciplinary Electives Offered to Other Department PG Students by Electronics and Communication Engineering Department

S.	Code	Course Name	Pre-requisite	Year
1.	ECE18R5141	Basics of VLSI Design	--	I
2.	ECE18R5142	CMOS IC Design	--	I
3.	ECE18R6141	Digital Design Using Verilog HDL	--	II

SCHEME OF INSTRUCTION

COURSE CODE	COURSE	L	T	P	C
MAT18R5001	Applied Mathematics	3	0	0	3
ECE18R5101	RTL Simulation and Synthesis with PLDs	3	0	0	3
ECE18R5102	Designing with ASICs	3	0	0	3
ECE18R5180	RTL Simulation and Synthesis with PLDs Laboratory	0	0	3	2
ECE18R5181	ASIC CAD Laboratory	0	0	3	2
ECE18R51XX	Program Specific Elective I	3	0	0	3
ECE18R51XX	Program Specific Elective II	3	0	0	3
AUD18RXXX	Audit Course I	2	0	0	0
PGM18R5001	Research Methodology for Engineers	0	1	0	1
ECE18R5103	Analog and Digital CMOS VLSI Design	3	0	0	3
ECE18R5104	VLSI Design Verification and Testing	3	0	0	3
ECE18R5182	Analog and Digital CMOS VLSI Design Laboratory	0	0	2	2
ECE18R5183	VLSI Design Verification and Testing Laboratory	0	0	2	2
ECE18R51XX	Program Specific Elective III	3	0	0	3
ECE18R51XX	Program Specific Elective IV	3	0	0	3
ECE18R5199	Mini Project	0	0	3	2
AUD18RXXX	Audit Course II	2	0	0	0
ECE18R6101	Microcontrollers and Programmable Digital Signal Processors	3	0	0	3
ECE18R61XX	Program Specific Elective V	3	0	0	3
XXX18RXXXX	Open Elective	3	0	0	3
ECE18R6198	Project Work Phase I	0	0	20	10
ECE18R6199	Project Work Phase II	0	0	32	16

AUD18R5001 ENGLISH FOR RESEARCH PAPER WRITING

AUD18R5001 English for Research Paper Writing

Course Category: Audit Course

COURSE OBJECTIVE(S):
To make students
Understand that how to improve their writing skills and level of readability
Learn about what to write in each section
Understand the skills needed when writing a Title
Ensure the good quality of paper at very first-time submission

COURSE OUTCOME(S):
At the end of the course, students will be able to:
CO1: Improve their communication skills in writing technical reports and articles
Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1						L	L	H	H	H		L			H

COURSE TOPICS:
UNIT 1
Planning and Preparation, Word Order, breaking up long sentences, Structuring Paragraphs and Sentences, Being Concise and Removing Redundancy, Avoiding Ambiguity and Vagueness.
UNIT 2
Clarifying Who Did What, highlighting your findings, Hedging and Criticising, Paraphrasing and Plagiarism, Sections of a Paper, Abstracts, Introduction
UNIT 3
Review of the Literature, Methods, Results, Discussion, Conclusions, The Final Check
UNIT 4
The key skills which are needed when writing a Title, key skills that are needed when writing an Abstract, key skills which are needed when writing an Introduction, skills needed when writing a Review of the Literature, skills needed when writing the Methods, skills needed when writing the Results, skills needed when writing the Discussion, skills needed when writing the Conclusions
UNIT 5
useful phrases, how to ensure paper is as good as it could possibly be the first- time submission

REFERENCE(S):
1. Goldbort R, “Writing for Science”, Yale University Press (2006)
2. Day R, “How to Write and Publish a Scientific Paper”, Cambridge University Press, 2006

3. Nicholas J. Higham, "Handbook of Writing for the Mathematical Sciences", SIAM, 1998
4. Adrian Wallwork, "English for Writing Research Papers", Springer, 2011

AUD18R5002PEDAGOGY STUDIES

AUD18R5002Pedagogy Studies
Course Category: Audit Course

COURSE OBJECTIVE(S):

To introduce students on

What pedagogical practices are being used by teachers in formal and informal classrooms in developing countries?

What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?

How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy?

COURSE OUTCOME(S):

At the end of the course, students will be able to:

CO1: Explain the various pedagogical practices and their effectives in formal and informal classrooms

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1						L	L	H	H	H		L			H

COURSE TOPICS:

UNIT 1

Introduction and Methodology: Aims and rationale, Policy background, Conceptual framework and terminology, Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions. Overview of methodology and Searching.

UNIT 2

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT 3

Evidence on the effectiveness of pedagogical practices, Methodology for the in-depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body of evidence for effective pedagogical practices.

UNIT 4

Professional development: alignment with classroom practices and follow- up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning limited resources and large class sizes

UNIT 5

Research gaps and future directions, Research design, Contexts, Pedagogy, Teacher education, Curriculum and assessment, Dissemination and research impact.

REFERENCE(S):

1. Ackers J, Hardman F (2001) Classroom interaction in Kenyan primary schools, Compare, 31 (2): 245-261
2. Agrawal M (2004) Curricular reform in schools: The importance of evaluation, Journal of Curriculum Studies, 36 (3): 361-379
3. Akyeampong K (2003) Teacher training in Ghana - does it count? Multi-site teacher education research project (MUSTER) country report 1. London: DFID
4. Akyeampong K, Lussier K, Pryor J, Westbrook J (2013) Improving teaching and learning of basic mathematics and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272-282
5. Alexander RJ, "Culture and Pedagogy: International Comparisons in Primary Education", Oxford University Press, 2001
6. Chavan M, "Read India: A mass scale, rapid, 'learning to read' campaign"
7. www.pratham.org/images/resource%20working%20paper%202.pdf

MAT18R5001 APPLIED MATHEMATICS

MAT18R5001 Applied Mathematics				
	L	T	P	C
	3	0	0	3
Pre-requisite: Basic Knowledge in UG Mathematics	**Course Category:** Supportive Course **Course Type:** Theory			

COURSE OBJECTIVE(S):

The main objective of this course is to demonstrate various analytical skills in applied mathematics and extensive experience with the tactics of problem solving and logical thinking applicable for engineering. This course will also help the students to identify, formulate, abstract and solve problems in engineering using mathematical tools from variety of mathematical areas, including matrix theory, probability, random variables, queueing theory, classical optimisation and linear programming.

COURSE OUTCOME(S):

After completing this course, the student will be able to:

CO1: Evaluate norms, generalized eigen vector, Pseudo Inverse and QR decomposition of a Matrix.

CO2: Understand the concept of probability, random variables, various probability distributions and its applications.

CO3: Apply the techniques of Queueing models in real life situations.

CO4: Understand the various concepts of classical optimisation techniques.

CO5: Apply graphical method, Simplex method and Dual Simplex method to solve LinearProgramming Problems and solving Transportation problems.

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	H	M		L		L							L		
CO2	H	H	L									L		H	
CO3	L	H		M											

COURSE TOPICS:

UNIT 1: MATRIX THEORY

Matrix Norms - Jordan Canonical form – Generalized Eigen vectors - Pseudo Inverse – QR-decomposition – QR Algorithm.

UNIT 2: PROBABILITY AND RANDOM VARIABLES

Probability – conditional probability - Random variables – Mathematical Expectation – Moments -Moment Generating function - Binomial, Poisson, Geometric, Uniform, Exponential and Normal Distributions – Function of a random variable.

UNIT 3: QUEUEING MODELS

Markovian Queues - Single and multi-server models – Little's formula - Steady state analysis – Queuing applications.

UNIT 4: CLASSICAL OPTIMISATION TECHNIQUES

Classification – optimisation technique - Unconstrained Optimisation – Equality constraints – Inequality constraints – Lagrange Multiplier method – Kuhn-Tucker Condition - Indirect search methods – Gradient of a function – Steepest descent method – Conjugate gradient method – Newton's method.

UNIT 5: LINEAR PROGRAMMING

Standard form of Linear programming problem – formation – graphical method - Simplex method – Dual simplex method – Transportation problem - Applications.

REFERENCE(S):

1. Bronson.R. "Matrix Operations", McGraw Hill, 2011 (2nd Edition).
2. Gupta S.C. and Kapoor V.K. "Fundamentals of Mathematical Statistics", Sultan Chand and Sons, 2014.
3. Taha H A, "Operations Research, An Introduction", Pearson, 2016 (9th Edition).
4. Singiresu S.Rao,"Engineering Optimization: Theory and Practice", New Age International, 2009 (4th Edition)
5. S.D. Sharma, "Operations Research", Kedar Nath Ram Nathand Company, 2008.
6. Sheldon M. Ross, "Probability and Statistics for Engineers and Scientists", Elsevier, 2011 (5th Edition)

PGM18R5001RESEARCH METHODOLOGY FOR ENGINEERS

PGM18R5001Research Methodology for Engineers				
	L	T	P	C
	0	1	0	1
Pre-requisite: -	**Course Category:** Supportive Course			

	Course Type: Theory

COURSE OBJECTIVE(S):

To formulate research problem and identify errors in research problem
To learn approaches for effective literature survey
To prepare presentation and research proposal

COURSE OUTCOME(S):

At the end of this course, students will be able to
CO1: To understand the basic concepts of research and its methodologies.
CO2: To select and define appropriate research problems.
CO3: To solve statistical problems and probability distributions.
CO4: To process and analysis the methods of data collection.
CO5: To recognise the powerfulness of the soft computing tools and to formulate the optimisation problems and write a research report, thesis and proposal

COURSE TOPICS:

UNIT 1: INTRODUCTION

Definition and objectives of Research – Types of research, Various Steps in Research process, Mathematical tools for analysis, developing a research question-Choice of a problem Literature review, Surveying, synthesizing, critical analysis, reading materials, reviewing, rethinking, critical evaluation, interpretation, Research Purposes, Ethics in research – APA Ethics code.

UNIT 2: QUANTITATIVE METHODS FOR PROBLEM SOLVING

Statistical modelling and analysis, time series analysis probability distributions, Fundamentals of statistical analysis and interference, multivariate methods, concepts of correlation and regression, fundamentals of time series, analysis and spectral analysis, error analysis, applications of spectral analysis.

UNIT 3: TABULAR AND GRAPHICAL DESCRIPTION OF DATA

Tables and graphs of frequency data of one variable, Tables and graphs that show the relationship between two variables, relation between frequency distributions and other graphs, preparing data for analysis.

UNIT 4: SOFT COMPUTING

Computer and its role in research, Use of statistical software SPSS, GRETL etc in research. Introduction to evolutionary algorithms- fundamentals of genetic algorithms, simulated annealing, and neural network-based optimisation, optimisation of fuzzy systems.

UNIT 5: REPORT WRITING

Structure and Components of Research Report, Types of Report, Layout of Research Report, Mechanism of writing a research report, referencing in academic writing

REFERENCE(S):

1. C.R. Kothari, "Research Methodology Methods and Techniques", VishwaPrakashan, 2009
2. Donald H.McBurney, "Research Methods", Thomson Learning,2009 (5th Edition)
3. Donald R.Cooper, Pamela S.Schindler, "Business Research Methods", McGraw Hill, 2011 (8th Edition).

4. Timothy J. Ross, "Fuzzy Logic with Engineering Applications", Wiley, 2014 (2nd Edition)
5. Van Laarhoven and E.H. Aarts (Editors), "Simulated Annealing: Theory and Applications (Mathematica and its applications)", Springer, 2013 (Reprint)
6. David E Goldberg, "Genetic Algorithms in Search, Optimization and Machine Learning", Pearson, 2013 (Reprint)

ECE18R5101RTL SIMULATION AND SYNTHESIS WITH PLDS

ECE18R5101 RTL Simulation and Synthesis with PLDs				
	L	**T**	**P**	**C**
	3	**0**	**0**	**3**
Pre-requisite Basic Electronics	**Course Category:** Program Core **Course Type:** Theory			

COURSE OBJECTIVE(S):
This course deals with design process flows, software tools and case studies of various FPGA architectures. In addition to that it also describes about synthesis, simulation, computational applications, business applications and recent development of FPGA market.

COURSE OUTCOME(S):
At the end of the course, students will demonstrate the ability to:
CO1: Familiarity of Finite State Machines, RTL design using reconfigurable logic.
CO2: Design and develop IP cores and Prototypes with performance guarantees
CO3: Use EDA tools like Cadence, Mentor Graphics and Xilinx.

Mapping of Course Outcome(s):

CO / PO	**PO**												**PSO**		
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
CO1	H	L	H	H	L	L			L		M	M	H		
CO2	H	H	H	M					L		L	M		H	
CO3	H	M	H	H	H	L					H	M		H	

COURSE TOPICS:
UNIT 1:
Design of FSMs (Synchronous and asynchronous), Static timing analysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.
UNIT 2:
Design entry by Verilog/VHDL/FSM, Verilog AMS.
UNIT 3:
Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning,Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.
UNIT 4:
Design for performance, Low power VLSI design techniques. Design for testability.
UNIT 5:
IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP,

Netlist, Physical IP, Use of external hard IP during prototyping

REFERENCE(S):

1. Richard S. Sandige, "Modern Digital Design", McGraw Hill, 2009 (Reprint)
2. Donald D Givone, "Digital principles and Design",McGraw Hill, 2009 (Reprint)
3. Charles Roth, Jr. and Lizy K John, "Digital System Design using VHDL",CengageLearning, 2016 (3rdEdition)
4. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson, 2015 (2ndEdition 2003 Reprint).
5. Doug Amos, Austin Lesea, Rene Richter, "FPGA Based Prototyping Methodology Manual: Best Practices in Design-for-Prototyping", Synopsys/Xilinx, 2011
6. Bob Zeidman, "Designing with FPGAs and CPLDs", CMP Books/Elsevier, 2011 (2002 Reprint)

ECE18R5102DESIGNING WITH ASICs

ECE18R5102 Designing with ASICs				
	L	**T**	**P**	**C**
	3	**0**	**0**	**3**
Pre-requisite: Basic Electronics	**Course Category:** Program Core **Course Type:** Theory			

COURSE OBJECTIVE(S):

The course focuses on the semi-custom IC Design and introduces the principles of design Logic cells, I/O cells and interconnect architecture and ASIC design flow is dealt with from the circuit and layout design point of view.

COURSE OUTCOME(S):

After completing this course, the student will be able to:

CO1: Understand the CMOS fundamentals and ASIC library design.

CO2: Apply appropriate techniques, resources and tools to engineering activities for appropriate solution to develop ASICs

CO3: Solve problems of Design issues, simulation and Testing of ASICs.

CO4: Able to design at the next transistor and block level abstractions of ASIC design

CO5: Demonstrate an understanding of algorithms related to ASIC design

Mapping of Course Outcome(s):

CO / PO	**PO**												**PSO**		
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
CO1	H		H	H	M	L			L		M	M	L		
CO2	H	L	H		H						H	M			H
CO3	H	H	H	L	H	L					H	H	H	M	
CO4	H	L	H	L					L		M	L			
CO5	H	L	L	M					M		M	L		H	

COURSE TOPICS:

UNIT 1: OVERVIEW OF ASICS

ASICs types, design flow, comparison, cell libraries, CMOS transistors, CMOS process, CMOS rules, combinational logic cells, sequential logic cells, data path logic cells, i/o cells, cell compilers, ASIC library design.

UNIT 2: LOGIC CELLS AND I/O CELLS

Anti-fuse, Static RAM, EPROM and EEPROM technology, Issues, Specifications, PREP benchmarks, Actel ACT, Xilinx LCA, Altera FLEX, Altera MAX, DC and AC I/Os, Clock input, Power input, Xilinx I/O blocks, Other I/O cells.

UNIT 3: ASIC ARCHITECTURE

Architecture and configuration of Spartan / Cyclone and Virtex/ Stratix FPGAs – Micro-Blaze / Nios based embedded systems – Signal probing techniques.

UNIT 4: LOGIC SYNTHESIS, PLACEMENT AND ROUTING

Logic synthesis - ASIC floor planning- placement and routing – power and clocking strategies

UNIT 5: ALGORITHMS FOR ASICS

DAA and computation of FFT and DCT. High performance filters using delta-sigma modulators. SoCCase Studies: Digital camera, SDRAM, High speed data standards

REFERENCE(S):

1. M.J. Sebastian Smith, “ApplicationSpecific – Integrated Circuits”, Pearson, 2011
2. Paul M.Jr.Brown “A Guide to Analog ASICs”, AcademicPress 2012
3. Steve Kilts, “Advanced FPGA Design: Architecture, Implementation and Optimization”,IEEE/ Wiley, 2007
4. Roger Woods, John McAllister, Dr. Ying Yi, Gaye Lightbod, “FPGA-based Implementationof Signal Processing Systems”, Wiley, 2008
5. Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing ",McGraw Hill, 1994
6. Douglas J. Smith, “HDL Chip Design: A Practical Guide for Designing, Synthesizing, and Simulating ASICs and FPGAs Using VHDL Or Verilog”, Doone Publications, 1996
7. Jose E. France, YannisTsividis, "Design of Analog - Digital VLSI Circuits forTelecommunication and Signal Processing", Prentice Hall, 1994

ECE18R5103 ANALOG AND DIGITAL CMOS VLSI DESIGN

ECE18R5103 Analog and Digital CMOS VLSI Design				
	L	**T**	**P**	**C**
	3	**0**	**0**	**3**
Pre-requisite: Linear Integrated Electronics	**Course Category:** Program Core **Course Type:** Theory			

COURSE OBJECTIVE(S):

To introduce the basic concepts of digital CMOS design and optimisation of various design parameters.

To familiarise the physical design algorithms for VLSI design.

To introduce short channel effects, FINEET and metal gate technology.

To familiarise differential amplifiers with various MOS loads and use of operational

amplifiers in analog design

COURSE OUTCOME(S):

At the end of this course, students will be able to

CO1: Analyse, design, optimise and simulate analog and digital circuits using CMOS constrained by the design metrics.

CO2: Connect the individual gates to form the building blocks of a system.

CO3: Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice.

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	H		L		L				L		L	M		H	
CO2	H	M	H	L							H	H	L	H	
CO3	H	H	L	H	M				L	L	H	H		M	L

COURSE TOPICS:

UNIT 1: CMOS REVIEW

Basic MOS structure and its static behaviour, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behaviour, Power consumption.

UNIT 2: PHYSICAL DESIGN FLOW

Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model, Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

UNIT 3: SEQUENTIAL LOGIC

Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-Bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High–k, Metal Gate Technology, FinFET, TFET etc.

UNIT 4: SINGLE STAGE AMPLIFIER

CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common-gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.

UNIT 5: PASSIVE AND ACTIVE CURRENT MIRRORS, OPERATIONAL AMPLIFIERS

Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise

One stage OPAMP, two stage OPAMP, gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.

REFERENCE(S):

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A Design Perspective", Pearson 2017 (Reprint)
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 1997
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2016 (2nd Edition)
4. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2012 (3rd Edition)
5. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE /Wiley, 2018(4th Edition)
6. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", McGraw Hill, 2014 (4th Edition)
7. Douglas A. Pucknell, Kamran Eshraghian, "Basic VLSI Design", PHI, 2008 (3rd Edition)

ECE18R5104 VLSI DESIGN VERIFICATION AND TESTING

ECE18R5104 VLSI Design Verification and Testing	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**
Pre-requisite: C Programming	**Course Category:** Program Core **Course Type:** Theory			

COURSE OBJECTIVE(S):
To introduce the concept of testbench functionality and various types of testbench.
To familiarise the various data types and use of data types in hardware description languages to develop digital system.
To introduce the subprograms: functions and procedures, use of subprograms in VLSI Testing
To familiarise the System Verilog, basic OOP, object creation and utilisation and randomisation in System Verilog.

COURSE OUTCOME(S):
At the end of this course, students will be able to
CO1: Familiarity of Front-end design and verification techniques and create reusable test environments.
CO2: Verify increasingly complex designs more efficiently and effectively.
CO3: Use EDA tools like Cadence, Mentor Graphics.
Mapping of Course Outcome(s):

CO / PO	**PO**												**PSO**		
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
CO1	H		L		L				L		L	M		H	
CO2	H	M	H	L							H	H	L	H	
CO3	H	H	L	H	M				L	L	H	H		M	L

COURSE TOPICS:
UNIT 1: TESTING
Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, Layered testbench, Building layered testbench, Simulation environment phases,

Maximum code reuse, Testbench performance.

UNIT 2: DATA TYPES

Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, choosing a storage type, creating new types with typedef, Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width.

UNIT 3: PROCEDURAL STATEMENTS AND ROUTINES

Procedural statements, tasks, functions and void functions, Routine arguments, returning from a routine, Local data storage, Time values Connecting the testbench and design: Separating the testbench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.

UNIT 4: SYSTEM VERILOG ASSERTIONS

Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Local, Straying off course building a testbench.

UNIT 5: RANDOMIZATION

Introduction, what to randomize, Randomization in System Verilog, Constraint details solution probabilities, controlling multiple constraint blocks, Valid constraints, In-line constraints, the pre_randomize and post_randomize functions,

Random number functions, Constraints tips and techniques, Common randomization problems, Iterative and array constraints, Atomic stimulus generation vs. Scenario generation, Random control, Random number generators, Random device configuration.

REFERENCE(S):

1. Chris Spear, Greg Tumbush, “System Verilog for Verification: A Guide to Learning the Testbench Language Features”, Springer, 2012 (3rd Edition)
2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing: For Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002
3. IEEE1800-2009Standard(IEEEStandardforSystem Verilog—UnifiedHardware Design, Specification, and Verification Language).
4. System Verilog website
   www.systemverilog.org
5. http://www.sunburstdesign.com/papers/CummingsSNUG2006Boston_SystemVerilogEvents.pdf
6. General reuse information and resources
   www.design-reuse.com
7. OVM, UVM (on top of SV)www.verificationacademy.com
8. Verification IP resources:
   http://www.cadence.com/products/fv/verification_ip/pages/default.aspx
   http://www.synopsys.com/Tools/Verification/FunctionalVerification/VerificationIP/Pages/default.aspx

ECE18R5180 RTL SIMULATION AND SYNTHESIS WITH PLDS LABORATORY

ECE18R5180 RTL Simulation and Synthesis with PLDs Laboratory	L	T	P	C
	0	0	3	2
Co-Requisite: ECE18R5101 RTL Simulation and Synthesis with PLDs	**Course Category:** Program Core **Course Type:** Laboratory			

COURSE OBJECTIVE(S):
To attain expertise in the domain of communication systems and signal processing with the help of RTL design tools.

COURSE OUTCOME(S):
At the end of the laboratory work, students will be able to:
CO1: Identify, formulate, solve and implement problems in signal processing, communication systems etc using RTL design tools.
CO2: Use EDA tools like Cadence, Mentor Graphics and Xilinx
Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1		M					L			M		H		M	
CO2	H	L			H	H	M	H	M		M	M	H	H	

LIST OF EXPERIMENTS:
1) Verilog implementation of 8:1 Mux/Demux, Full Adder, 8-bit Magnitude comparator, Encoder/decoder, Priority encoder, D-FF, 4-bit Shift registers (SISO, SIPO, PISO, bidirectional), 3-bit Synchronous Counters, Binary to Gray converter, Parity generator.
2) Sequence generator/detectors, Synchronous FSM – Mealy and Moore machines.
3) Vending machines - Traffic Light controller, ATM, elevator control.
4) PCI Bus arbiter and downloading onFPGA.
5) UART/ USART implementation inVerilog.
6) Realization of single port SRAM inVerilog.
7) Verilog implementation of Arithmetic circuits like serial adder/ subtractor, parallel Adder/subtractor, serial/parallelmultiplier.
8) Discrete Fourier transform/Fast Fourier Transform algorithm inVerilog.

ECE18R5181 ASIC CAD LABORATORY

ECE18R5181ASIC CAD Laboratory	L	T	P	C
	0	0	3	2
Pre-requisite: ECE18R5102Designing with ASICs	**Course Category:** Program Core **Course Type:** Laboratory			

COURSEOBJECTIVE (S):

Exposure to various stages of a typical state of the art CAD VLSI tool be provided by various experiments designed to bring out the key aspects of each important module in the CAD tool including the synthesis, place and route, layout, LVS, simulation, and power and clock routing modules.

COURSE OUTCOME(S):
After completing this course, the student will be able to:
CO1: Able to carry out a complete VLSI based experiments using / CADENCE / TANNER /Mentor/Synopsis
CO2: Able to design and carry out Static timing analyses of simple digital building blocks
CO3: Work as part of a team and as individual effectively in designing simple circuits following the safety procedures and ethics
CO4: Communicate technical information related to custom design by means of oral and written reports

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	H	H	H	M	H	M	M	M	M	M	L	M	H	H	
CO2	H	H	H	M	H	M	M	M	M	M	L	M	H	H	
CO3						H	H	H	H	M		L			
CO4						M	M	H	M	H		L			H

LIST OF EXPERIMENTS:
CAD Tool Familiarization-CADENCE/SYNOPSYS/MENTOR GRAPHICS (or equivalent) and PSPICE.
Digital Circuit Simulation and synthesis
To simulate, synthesize and understand the Boolean optimisation in synthesis. Static timing analyses procedures and constraints. Critical path considerations. Scan chain insertion, Floor planning, Routing and Placement procedures. Power planning, Layout generation, LVS and back annotation, C power estimate.
Analog circuit simulation.
Simulation of logic gates, Current mirrors, Current sources, Differential amplifier in Spice. Layout generations, LVS, Back annotation

ECE18R5182 ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY

ECE18R5182 Analog and Digital CMOS VLSI Design Laboratory	L	T	P	C
	0	0	3	2
Co-requisite: ECE18R5103 Analog and Digital CMOS VLSI Design	**Course Category:** Program Core **Course Type:** Laboratory			

COURSE OBJECTIVE(S):
To introduce the basic concepts of digital CMOS design and optimisation of various design parameters.

To familiarise the physical design algorithms for VLSI design.
To introduce short channel effects, FINEET and metal gate technology.
To familiarise differential amplifiers with various MOS loads and use of operational amplifiers in analog design

COURSE OUTCOME(S):
At the end of the laboratory work, students will be able to:
CO1: Design digital and analog Circuit using CMOS.
CO2: UseEDAtoolslikeCadence,Mentor GraphicsandotheropensourcesoftwaretoolslikeNgspice.

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1		M					L			M		H		M	
CO2	H	L			H	H	M	H	M		M	M	H	H	

LIST OF EXPERIMENTS:

1) Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOSProcess.
   (a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
   (b) Plot ID vs. VGS at drain voltage (low) for NMOS, PMOS and determine Vt.
   (c) Plot log ID vs. VGS at gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
   (d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
   (e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS = 30mV
   To extract Vth, use the following procedure.
   (i) Plot gmvs VGS using NGSPICE and obtain peak gmpoint.
   (ii) Plot y=ID/(gm)1/2 as a function of VGS usingNgspice.
   (iii) Use Ngspicetoplot tangent line passing through peak gm point in y (VGS) plane and determineVth.
   (f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gainfrequency.
   Tabulate your result according to technologies and comment on it.
2) Use VDD=1.8V for 0.18um CMOS process, VDD=1.2V for 0.13um CMOS Process and VDD=1V for 0.09um CMOSProcess.
   (a) Perform thefollowing
   (i) Plot VTC curve for CMOS inverter and thereon plot dVoutvs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for theinverter.
   (ii) Plot VTC for CMOS inverter with varyingVDD.
   (iii) Plot VTC for CMOS inverter with varying deviceratio.
   (b) Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% trand 80%-to-20% tf. (use VPULSE = 2V, Cload =50fF)
   (c) Perform AC analysis of CMOS inverter with fanout 0 and fanout1. (Use Cin=

0.012pF, Cload = 4pF, Rload =k)

3) Use Ngspicetobuild a three stage and five stage ring oscillator circuit in 0.18um and 0.13um technology and compare its frequencies and timeperiod.

4) Perform thefollowing

(a) Draw small signal voltage gain of the minimum-size inverter in 0.18um and 0.13um technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18um and 0.13umprocess.

(b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18um technology. (W/L) MN=5, (W/L) MP=10 and L=0.5um for both transistors.

(i) Establish a test bench, as explained in the lecture, to achieveVDSQ=VDD/2.

(ii) Calculate input bias voltage if biascurrent=50uA.

(iii) Use Ngspice and obtain the bias current. Compare its value with50uA.

(iv) Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).

(v) Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dBBW

(vi) Use Ngspice to determine input voltage range of theamplifier

5) Three OPAMP INA.Vdd=1.8V Vss=0V, CAD tool: MentorGraphicsDA.Note: Adjust accuracy options of the simulator (setup->options inGUI).Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

(a) Draw the schematic of op-amp macro model.

(b) Draw the schematic of INA.

(c) Obtain parameters of the op-amp macro model such that

low-frequency voltage gain =5 x 104,
unity gain BW (fu) =500 kHz,
input capacitance=0.2pF,
output resistance =,
CMRR=120 dB

(d) Draw schematic diagram of CMRR simulation setup.

(e) Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

(f) Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.

(g) Repeat (c) to (f) by considering CMRR of all OPAMP to be 90dB.

6) Technology: UMC 0.18um, VDD=1.8V. Use MAGIC or Micro wind.

(a) Draw layout of a minimum size inverter in UMC 0.18um technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.

(b) Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.

(c) Use extracted netlist and obtain tPHL tPLH for the middle inverter using Eldo.
(d) Use interconnect length obtained and connect the second and third inverter. Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delay times with corresponding values obtained in part 'c'.

ECE18R5183 VLSI DESIGN VERIFICATION AND TESTING LABORATORY

ECE18R5183 VLSI Design Verification and Testing Laboratory	L	T	P	C
	0	0	3	2
Co-Requisite: ECE18R5104 VLSI Design Verification and Testing	**Course Category:** Program Core **Course Type:** Laboratory			

COURSE OBJECTIVE:
To obtain expertise in designing complex circuits using Electronic Design Automation, and gaining more knowledge in tools like Cadence, Mentor Graphics.

COURSE OUTCOME(S):
At the end of the laboratory work, students will be able to:
CO1: Verify increasingly complex designs more efficiently and effectively.
CO2: Use EDA tools like Cadence, Mentor Graphics.
Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1		M					L			M		H		M	
CO2	H	L			H	H	M	H	M		M	M	H	H	

LIST OF EXPERIMENTS:
1. Sparse memory
2. Semaphore
3. Mailbox
4. Classes
5. Polymorphism
6. Coverage Assertion

ECE18R5199MINI PROJECT

ECE18R5199Mini Project	L	T	P	C
	0	0	3	2
Pre-requisite: -	**Course Category:** Project **Course Type:** Laboratory			

COURSE OBJECTIVE(S):

Ability to synthesise knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem
Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design
Ability to present the findings of their technical solution in a written report.

COURSE OUTCOME(S):
At the end of the course, students will be able to:
CO1: Apply the gained knowledge and skills to solve new technical problems
CO2: Select from different methodologies, methods and analysis forms to produce a suitable research design and justify their design
CO3: Present their proposed solution by oral and written reports
CO4: Manage and execute the projects of solving technical problems
Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	H	H	H	M	M							H	H		
CO2			M	H	H	M	L					H	H		
CO3								H	H	H					H
CO4						L	M	L	L	H	H	L		H	

SYLLABUS:
The mini project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study.
The dissertation should have the following

- Relevance to social needs of society
- Relevance to value addition to existing facilities in the institute
- Relevance to industry need
- Problems of national importance
- Research and development in various domain

The student should complete the following:

- Literature survey Problem Definition
- Motivation for study and Objectives
- Preliminary design / feasibility / modular approaches
- Implementation and Verification
- Report and presentation

ECE18R6101 MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

ECE18R6101 Microcontrollers and Programmable Digital Signal Processors	L	T	P	C
	3	0	0	3
Pre-requisite: Microprocessors and Digital Signal Processing	**Course Category:** Program Core **Course Type:** Theory			

COURSE OBJECTIVE(S):

To know programming model of ARM and learn instructions of ARM.
To learn about interrupt, timer, memory and peripherals of ARM.
To know about DSP architecture and learn programming.
To learn application development of DSP

COURSE OUTCOME(S):

At the end of this course, students will be able to

CO1: Compare and select ARM processor core based SoC with several features/peripherals based on requirements of embedded applications.

CO2: Identify and characterize architecture of Programmable DSPProcessors

CO3: Develop small applications by utilizing the ARM processor core and DSP processor-based platform.

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1		M					L			M		H		M	
CO2	H	L			H	H	M	H	M		M	M	H	H	
CO3		L			H	L	L	H	M			M			L
CO4	H	L	H	H		L	M	H	M	M		M	L		
CO5						H	H	H	H	M		L			
CO6						M	M	H	M	H		L			H

COURSE TOPICS:

UNIT 1

Applications, Programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence Instruction Set, Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces

UNIT 2

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pend able Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT 3

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT

UNIT 4

Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

UNIT 5

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.

Code Composer Studio for application development for digital signal processing, On chip peripherals, Processor benchmarking.

REFERENCE(S):

1. Joseph Yiu, "The Definitive Guide to ARM Cortex-M3", Elsevier / Newnes, 2011 (2007 Reprint)
2. Venkataramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications",McGraw Hill, 2008 (Reprint)
3. Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide: Designing and Optimizing System Software", Morgan Kaufman / Elsevier, 2004
4. Steve Furber, "ARM System-on-Chip Architecture", Pearson, 2009 (2nd Edition)
5. Frank Vahid and Tony Givargis, "Embedded System Design: A Unified Hardware/Software Introduction", Wiley, 2009 (Reprint)
6. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instrumentswww.ti.com.

ECE18R6198 PROJECT WORK PHASE I

ECE18R6198 Project Work Phase I	L	T	P	C
	0	0	20	10
Pre-requisite: -	**Course Category:** Project **Course Type:** Laboratory			

COURSE OBJECTIVE(S):

Ability to synthesise knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem

Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design

Ability to present the findings of their technical solution in a written report.

COURSE OUTCOME(S):

At the end of the course, students will be able to:

CO1: Apply the gained knowledge and skills to solve new technical problems

CO2: Select from different methodologies, methods and analysis forms to produce a suitable research design and justify their design

CO3: Present their proposed solution by oral and written reports

CO4: Manage and execute the projects of solving technical problems

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	H	H	H	M	M							H	H		
CO2			M	H	H	M	L					H	H		
CO3								H	H	H					H
CO4						L	M	L	L	H	H	L		H	

SYLLABUS:

The dissertation / project topic should be selected / chosen to ensure the satisfaction of the urgent need to establish a direct link between education, national development and productivity and thus reduce the gap between the world of work and the world of study.
The dissertation should have the following

- Relevance to social needs of society
- Relevance to value addition to existing facilities in the institute
- Relevance to industry need
- Problems of national importance
- Research and development in various domain

The student should complete the following:

- Literature survey Problem Definition
- Motivation for study and Objectives
- Preliminary design / feasibility / modular approaches
- Implementation and Verification
- Report and presentation

Phase – I deliverables: A document report comprising of

- summary of literature survey,
- detailed objectives,
- project specifications,
- paper and/or computer aided design,
- proof of concept/functionality,
- part results,
- record of continuous progress.

ECE18R6199 PROJECT WORK PHASE II

ECE18R6199 Project Work Phase II	L	T	P	C
	0	0	32	16
Pre-requisite:ECE6198 Project Work Phase I	**Course Category:** Project **Course Type:** Laboratory			

COURSE OBJECTIVE(S):
Ability to synthesise knowledge and skills previously gained and applied to an in-depth study and execution of new technical problem
Capable to select from different methodologies, methods and forms of analysis to produce a suitable research design, and justify their design
Ability to present the findings of their technical solution in a written report.
Presenting the work in International/ National conference or reputed journals.

COURSE OUTCOME(S):
At the end of the course, students will be able to:
CO1: Apply the gained knowledge and skills to solve new technical problems
CO2: Select from different methodologies, methods and analysis forms to produce a suitable research design and justify their design
CO3: Present their proposed solution by oral and written reports and submit their works in conference/journal

CO4: Manage and execute the projects of solving technical problems

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
CO1	H	H	H	M	M							H	H		
CO2			M	H	H	M	L					H	H		
CO3								H	H	H					H
CO4						L	M	L	L	H	H	L		H	

SYLLABUS:

During phase – II, student is expected to exert on design, development and testing of the proposed work as per the schedule. Accomplished results/contributions/innovations should be published in terms of research papers in reputed journals and reviewed focused conferences or IP/Patents.

Phase – II deliverables: A document report comprising of

- summary of literature survey,
- detailed objectives,
- project specifications,
- paper and/or computer aided design,
- proof of concept/functionality,
- results, developed system in the form of hardware and/or software,
- record of continuous progress.

ECE18R5120NETWORK SECURITY AND CRYPTOGRAPHY

ECE18R5120Network Security and Cryptography				
	L	T	P	C
	3	0	0	3
Pre-requisite: Basics of Computer Communication and Networks	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):
To introduce basic and advanced concepts of security
To introduce various cryptography techniques
To teach students various authentication techniques
To introduce various threats

COURSE OUTCOME(S):
After completing this course, the student will be able to:
CO1: Identify and utilize different forms of cryptography techniques.
CO2: Incorporate authentication and security in the network applications
CO3: Distinguish among different types of threats to the system and handle the same
Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	H	H	L		L	L									
CO2	H	M	H	M	L	L					M	M	L		L
CO3	H	M	H	M	L	L					M	M		L	

COURSE TOPICS:
UNIT 1:
Security need, Security services, Attacks, OSI Security Architecture, one-time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques
Number Theory - Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic
UNIT 2:
Private-Key (Symmetric) Cryptography – Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA,Linear and Differential Cryptanalysis
UNIT 3:
Public-Key (Asymmetric) Cryptography - RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC
UNIT 4:
Authentication - IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer and Transport Layer Security, Secure Electronic Transaction

UNIT 5:
System Security - Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Firewall Design Principles, Trusted Systems

REFERENCE(S):

1. WilliamStallings,"Cryptography and Network Security: Principles and Practices",Pearson, 2016 (7th Edition)
2. Radia Perlman, Charlie Kaufman, Mike Speciner, "Network Security: PRIVATE Communication in a PUBLIC World", Pearson, 2017 (2nd Edition)
3. Christopher M. King, Curtis E. Dalton, T. Ertem Osmanoglu, "Security Architecture: Design, Deployment, and Operations", McGraw Hill, 2001
4. Stephen Northcutt, Lenny Zeltser, Scott Winters, Karen Kent, Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson, 2006 (2nd Edition)
5. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", No Starch Press, 2013

ECE18R5121 SEMICONDUCTOR DEVICE MODELLING

ECE18R5121 Semiconductor Device Modelling	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**
Pre-requisite Electron Devices	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):
The course will provide adequate understanding of semiconductor device modelling aspects useful for designing devices in electronic, and optoelectronic applications

COURSE OUTCOME(S):
After completing this course, the student will be able to:
CO1: Formulate problem in terms of finite elements
CO2: Develop compact models for Laser diodes.
CO3: Develop compact models for MESFET.
CO4: Understand and utilize the basic Quantum Physics to analyse semiconductor devices.
CO5: Utilize semiconductor models to analyse Quantum effects in device modelling.

Mapping of Course Outcome(s):

CO / PO	**PO**												**PSO**		
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**1**	**2**	**3**
CO1	H	H	L		L	L									
CO2	H	M	H	M	L	L					M	M	L		L
CO3	H	M	H	M	L	L					M	M		L	
CO4	H	M	L	M	H						H	M			
CO5	H	L		L							H	M	H		L

COURSE TOPICS:
UNIT 1: INTRODUCTION TO NUMERICAL MODELLING

Fundamental semiconductor equations, Finite difference scheme, Error analysis, Solution of a system of Linear Equations, Direct Method: LU-decomposition, Tri-diagonal system, Relaxation Method, Numerical solution of Non-Linear Equations: Newton-Raphson method, Finite difference discretization example: Current continuity and energy relations, Introduction to circuit simulations

UNIT 2: MODELLING OF LASER DIODE

Rate equations, Numerical schemes: Small signal modelling, and Large signal modelling, Equivalent circuits

UNIT 3: MESFET MODELLING

Bridging between time and frequency domains: Harmonic Balance Method, MESFET small signal and large signal equivalent circuit, numerical device simulation and parameter extraction

UNIT 4: QUANTUM PHYSICS ASPECTS OF DEVICE MODELLING

Effective mass Schrödinger equation, Matrix representation, Dirac notation, WKB Approximation, Time dependent and independent perturbation theories, Fermi's golden rule, semi-classical transport in semiconductors: Boltzmann transport equation, numerical scheme, Introduction to Monte Carlo simulations

UNIT 5: QUANTUM EFFECT DEVICE MODELLING

Double barrier resonant tunnelling diode, Device modelling through transfer matrix approach, Numerical estimation of diode current density, coupled Poisson-Schrödinger scheme for electron transmission simulations

REFERENCE(S):

1. Selberherr, S, "Analysis and Simulation of Semiconductor Devices", Springer, 1984
2. Christopher M Snowden, "Semiconductor Device Modelling", Springer, 2012
3. Arora, N, "MOSFET Models for VLSI Circuit Simulation", Springer, 1993
4. C.M. Snowden, and E. Snowden, "Introduction to Semiconductor Device modelling", World Scientific, 1998

ECE18R5122SCRIPTING LANGUAGES FOR VLSI DESIGN AUTOMATION

ECE18R5122 Scripting Languages for VLSI Design Automation	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**
Pre-requisite: ECE18R535 Physical Design Automation	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):

Scripting languages are used for automating tasks of different EDA tools. This course deals with programming with Scripting languages such as PERL, CGI, JAVA script, TCL and other languages such as python, ruby etc

COURSE OUTCOME(S):

After completing this course, the student will be able to:

CO1: Interpret typical scripting languages for system applications

CO2: Create software systems using Perl and Python
CO3: Understand the concepts of TCL
CO4: Develop Java script, python-based web system design.

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	H		L		H								M		
CO2			M		L				L			M		H	
CO3	M	L	L												
CO4	H		H		H				L			M	M	M	

COURSE TOPICS:

UNIT 1: SCRIPTING LANGUAGES

Definition of script, Scripting Context, Shell scripts Overview of Scripting Languages – PERL, CGI, VB Script, Java Script, Python, Ruby, and TCL

UNIT 2: PERL, INTERFACING

Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation and Line Interfacing

UNIT 3: PROGRAMMING IN PERL

Debugger Internal and Externals Portable Functions, Extensive Exercises for Programming in PERL, TCL language basics

UNIT 4: PROGRAMMING IN TCL, OTHER LANGUAGES

Basic commands, Control constructs, Advanced constructs, File I/O, TCL application in EDA tools, tk and wish, Example: Back Annotating a Verilog module, Broad Details of CGI, VB Script, Java Script, Python, Ruby with Programming Examples

UNIT 5: LINUX SHELL SCRIPTING

Parameters, making executable script, storing shell scripts, shell variables, editing documents with ed, editing documents with ed-Parameters, shell variables, debugging shell scripts, loops, variable modifiers-if, else, command line arguments-reading from standard input, using an output from a com-mand, switch

REFERENCE(S):

1. Randal L, Schwartz Tom Phoenix, “Learning PERL”, O’Reilly, 2016.
2. Tom Christiansen, Nathan Torkington, “PERL Cookbook”,O’Reilly, 2004.
3. Larry Wall, “Programming PERL”, O’Reilly, 2000.

ECE18R5123 VLSI SIGNAL PROCESSING

ECE18R5123 VLSI Signal Processing	L	T	P	C
	3	0	0	3
Pre-requisite: Digital Signal processing	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):

This course discusses about VLSI architectures for signal processing, techniques of critical path and algorithmic strength reduction in the filter structures and about the study of performance parameters, viz. Area, speed and power

COURSE OUTCOME(S):

At the end of this course, students will be able to

CO1: Acquired knowledge about DSP algorithms, its DFG representation, pipelining and parallel processing approaches.

CO2: Ability to acquire knowledge about retiming techniques, folding and register minimization path problems.

CO3: Ability to have knowledge about algorithmic strength reduction techniques and parallel processing of FIR and IIR digital filters.

CO4: Acquired knowledge about finite word-length effects and round off noise computation in DSPsystems.

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			L		L							H			
CO2	L		H		M	L		L				L		H	L
CO3	M	L	H		L			L				H		M	M
CO4	L		M		H								H		L

COURSE TOPICS:

UNIT 1

Introduction to DSP systems, Pipelined and parallel processing.

UNIT 2

Iteration Bound, Retiming, unfolding, algorithmic strength reduction in filters and Transforms.

UNIT 3

Systolic architecture design, fast convolution, pipelined and parallel recursive and adaptive filters, Scaling and round off noise.

UNIT 4

Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic.

UNIT 5

Numerical strength reduction, synchronous, wave and asynchronous pipelines, low power design.Programmable digit signal processors.

REFERENCE(S):

1. KeshabK.Parhi, “VLSI Digital Signal Processing Systems, Design and Implementation”, Wiley, 2007
2. U. Meyer, Baese, "Digital Signal Processing with Field Programmable Arrays", Springer, 2007 (2nd Edition)
3. S.Y.Kuang, H.J. White house, T. Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1995
4. V. K. Madisetti, “VLSI Digital Signal Processors: An Introduction to Rapid Prototyping and Design Synthesis”, IEEE Press, 1995

ECE18R5124 PARALLEL PROCESSING

ECE18R5124Parallel Processing				
	L	T	P	C
	3	0	0	3
Pre-requisite: Computer Architecture	**Course Category:** Program SpecificElective **Course Type:** Theory			

COURSE OBJECTIVE(S):

This course discusses about VLSI architectures for signal processing, techniques of critical path and algorithmic strength reduction in the filter structures and about the study of performance parameters, viz. Area, speed and power

COURSE OUTCOME(S):

At the end of this course, students will be able to

CO1: Identify limitations of different architectures of computer

CO2: Analysis quantitatively the performance parameters for different architectures

CO3: Investigate issues related to compilers and instruction set based on type of architectures.

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	L	L	L		L			H	M		L	L			
CO2	L	L	L		L			H	M		L	L	H	H	
CO3	L	L	L		L			H	M		L	L	L		

COURSE TOPICS:

UNIT 1

Overview of Parallel Processing and Pipelining, Performance analysis, Scalability

UNIT 2

Principles and implementation of Pipelining, Classification of pipelining, processors,Advancedpipelining techniques, Software pipelining

UNIT 3

VLIW PROCESSORS Case study: Superscalar Architecture- Pentium, Intel Itanium Processor, Ultra SPARC, MIPS onFPGA, Vector and Array Processor, FFT Multiprocessor Architecture

UNIT 4

Multithreaded Architecture, Multithreaded processors, Latency hiding techniques,Principles of multithreading, Issues and solutions

UNIT 5

Parallel Programming Techniques:Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues

REFERENCE(S):

1. Kai Hwang, FayéAlayé Briggs, "Computer Architecture and Parallel Processing", McGraw Hill, 1984
2. Kai Hwang, Naresh Jotwani, "Advanced Computer Architecture: Parallelism, Scalability, Programmability",McGraw Hill, 2016 (3rd Edition)
3. V. Rajaraman, L. Sivaram Murthy, "Parallel Computers: Architecture and Programming",PHI, 2016 (2nd Edition)
4. William Stallings, "Computer Organization and Architecture: Designing for Performance" Pearson, 2015 (10th Edition)
5. Kai Hwang, ZhiweiXu, "Scalable Parallel Computing",McGraw Hill, 1998
6. David Harris and Sarah Harris, "Digital Design and Computer Architecture", Morgan Kaufmann, 2007

ECE18R5125 SUBMICRON TECHNOLOGY

ECE18R5125 Submicron Technology	L	T	P	C
	3	0	0	3
Pre-requisite: ECE18R5131 Low Power VLSI Design	**Course Category**: Program Specific Elective **Course Type**: Theory			

COURSE OBJECTIVE(S):

This course describes about the concepts of CMOS devices at deep sub-micron level, necessity and concepts of low power design, design reliability and limitations of sub-micron technology since with technology scaling, the transistor density increased tremendously follow the Moore's law.

COURSE OUTCOME(S):

After completing this course, the student will be able to:

CO1: Understand the Concepts of silicon realization of ASIC and CMOS devices atdeep Submicron Level.

CO2: Apply the deep Submicron concepts to CMOS low power devices

CO3: Discuss about RF CMOS transistor sizing and its limitations.

CO4: Understand about the design constraints for CMOS devices at deep submicronlevel for low power and high speed

CO5: Understand about the reliability constraints while designing CMOS devices atsubmicron level.

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	L	L	L		L			H	M		L	L			
CO2	L	L	L		L			H	M		L	L	H	H	
CO3	L	L	L		L			H	M		L	L	L		
CO4	L	L	L		L			H	M		L	L		L	
CO5	L	L	L		L			H	M		L	L	L		

COURSE TOPICS:

UNIT 1: SILICON REALISATION OF ASIC

Handcrafted layout implementation-bit-slice layout implementation-Cell based layout implementation- gate array layout implementation-Hierarchical design approach- The choice of layout implementation form

UNIT 2: LOW POWER DESIGN

Sources of CMOS power consumption-technology options for low power-reduction of Pleak by technological measures Reduction of P-dyn by technology measures-reduction of P-dyn by reduced voltage process-design option for low power-computing power vs chip power-a scaling perspectives.

UNIT 3: DESIGN FOR RELIABILITY

Latch up in CMOS circuits-Electrostatics discharge-and its protection-Electro Migration Hot carrier degradation design for signal integrity-clock distribution and critical timing issues-clock generation and synchronization in different domain on a chip-the influence of interconnection design organization

UNIT 4: DEEP SUB-MICRON

RF CMOS Transistor downsizing limitations-. RF basic blocks layout implementation Submicron technology and layout dependent effects-input output interfacing, the bonding pad, the pad ring, electrostatic discharge prevention

UNIT 5: CMOS DEVICES

Clamp CMOS devices, Zener diode-input structure-output structure-pull up-pull down-i/o pad, power clamp-core/pad limitation I/O Pad description using Ibis-Connecting to the package-Signal propagation between integrated circuits

REFERENCE(S):

1. Harry J. M. Veendrick “Deep-Submicron CMOS ICs: From Basics to Asics”, Kluwer, 2000.
2. W. Nebel, Jean P. Mermet “Low Power Design in Deep Submicron Electronics”, Kluwer, 1997.
3. Van Der Meer, Arie van Staveren, Arthur H. M. van Roermund “Low-Power Deep Sub-Micron CMOS Logic: Sub-threshold Current Reduction”, Kluwer, 2004.

ECE18R5126VLSI INTERCONNECTS AND ITS DESIGN TECHNIQUES

ECE18R5126 VLSI Interconnects and its Design Techniques	**L**	**T**	**P**	**C**
	3	**0**	**0**	**3**
Pre-requisite: ECE18R5135 Physical Design Automation	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):

To gain knowledge on VLSI Interconnects by getting an insight on Transmission line parameters of VLSI interconnects and the novel solutions

COURSE OUTCOME(S):

After completing this course, the student will be able to:

CO1: Understand the concept of VLSI Interconnects
CO2: Analyse the Transmission line parameters of VLSI interconnects
CO3: Understand the novel solutions for interconnect problems

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	H										L		M		
CO2	H	M	H				L				M	L		H	
CO3	H		H	M									L		

COURSE TOPICS:

UNIT 1: PRELIMINARY CONCEPTS OF VLSI INTERCONNECTS

Interconnects for VLSI applications-copper interconnections –method of images- method of moments- even and odd capacitances- transmission line equations- miller's theorem-Resistive interconnects as ladder network- Propagation modes in micro strip interconnects-slow wave propagations- Propagation delay.

UNIT 2: PARASITIC RESISTANCES, CAPACITANCE AND INDUCTANCES

Parasitic resistances, capacitances and inductances- approximate formulas for inductances-green's function method: using method of images and Fourier integral approach- network analog method- Inductance extraction using fast Henry- copper interconnections for resistance modelling.

UNIT 3: INTERCONNECTION DELAYS

Metal insulator semiconductor micro strip line- transmission line analysis for single level interconnections- transmission line analysis for parallel multilevel interconnections- analysis of crossing interconnections- parallel interconnection models for micro strip line- modelling of lossy parallel and crossing interconnects- high frequency losses in micro strip line-Expressions for interconnection delays- Active interconnects.

UNIT 4: CROSS TALK ANALYSIS

Lumped capacitance approximation- coupled multi conductor MIS micro strip line model for single level interconnects- frequency domain level for single level interconnects-transmission line level analysis of parallel multi-level interconnections.

UNIT 5: NOVEL SOLUTIONS FOR PROBLEMS IN INTERCONNECTS

Optical interconnects – carbon Nano tubes / Graphene vs. Copper wires.

REFERENCE(S):

1. Michel S. Naksla, Q.J. Zhang, "Modelling and Simulation of High-speed VLSI Interconnects", Springer, 2012.
2. H B Bakog Lu, "Circuits, Interconnections and Packaging for VLSI", Addison Wesley, 1990.
3. J A Davis, J D Meindl, "Interconnect Technology and Design for Gigascale Integration", Kluwer, 2003.
4. Nurmi J, Tenhumen H, Isoaho J, Jantsch A, "Interconnect Centric Design for Advanced SOC and NOC", Springer, 2004.
5. C K Cheng, J Lillis, S Lin, N Chang, "Interconnect Analysis and Synthesis", Wiley, 2000.
6. Askok K Goel, "High speed VLSI Interconnections", Wiley, 2007.

ECE18R5127CAD OF DIGITAL SYSTEM

ECE18R5127CAD of Digital System	L	T	P	C
	3	0	0	3
Pre-requisite: ECE18R5135 Physical Design Automation	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):
To introduce different VLSI design methodologies.
To introduce VLSI automation tools.
To learn the basics of general-purpose methods for optimisation.
To learn the concept of simulation and synthesis of simple circuits using RTL

COURSE OUTCOME(S):
At the end of this course, students will be able to
CO1: Explain fundamentals of CAD tools for modelling, design, test and verification of VLSIsystems.
CO2: Explain various phases of CAD, including simulation, physical design, test and verification.
CO3: Demonstrate knowledge of computational algorithms and tools forCAD.
Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	H										L		M		
CO2	H	M	H				L				M	L		H	
CO3	H		H	M									L		

COURSE TOPICS:
UNIT 1
Introduction to VLSI Methodologies – Design and Fabrication of VLSI Devices, FabricationProcess and its impact on Design.
UNIT 2
VLSI design automation tools – Data structures and basic algorithms, graph theory and computational complexity, tractable and intractable problems.
UNIT 3
General purpose methods for combinational optimisation – partitioning, floor planning and pin assignment, placement, routing.
UNIT 4
Simulation – logic synthesis, verification, high level Synthesis.
UNIT 5
MCMS-VHDL-Verilog-implementation of simple circuits using VHDL

REFERENCE(S):
1. Naveed A. Sherwani, “Algorithms for VLSI Physical Design Automation”, Springer, 2009 (1993 Reprint)

2. Sabih H. Gerez, "Algorithms for VLSI Design Automation", Wiley, 2008 (1998 Reprint)

ECE18R5128PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE

ECE18R5128Programming Languages for Embedded Software	L	T	P	C
	3	0	0	3
Pre-requisite: C Programming	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):
To introduce about the 'C' programming language for handling different hardware.
To introduce about the OOP language.
To introduce about the CPP programming language for controlling hardware.
To introduce about the language scripting for handling data pattern

COURSE OUTCOME(S):
At the end of this course, students will be able to
CO1: Write an embedded C application of moderate complexity.
CO2: Develop and analyse algorithms inC++.
CO3: Differentiate interpreted languages from compiled languages.
Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	L	L	L		L			H	M		L	L			
CO2	L	L	L		L			H	M		L	L	H	H	
CO3	L	L	L		L			H	M		L	L	L		

COURSE TOPICS:
UNIT 1: EMBEDDED 'C' PROGRAMMING
Bitwise operations, Dynamic memory allocation, OSservices, Linked stack and queue, Sparse matrices, Binary tree, Interrupt handling in C, Code optimisation issues, Writing LCD drives, LED drivers, Drivers for serial port communication, Embedded Software Development Cycle and Methods(Waterfall, Agile)
UNIT 2: OBJECT ORIENTED PROGRAMMING
Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism
UNIT 3: CPP PROGRAMMING
'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation
UNIT 4: OVERLOADING AND INHERITANCE
Need of operator overloading, overloading the assignment, overloading using friends, type

conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions,

UNIT 5: TEMPLATES, SCRIPTING LANGUAGES

Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code:try-catch-throw,Multiple Exceptions.

Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation and Line Interfacing.

REFERENCE(S):

1. Michael J. Pont, "Embedded C", Pearson Education, 2008 (2nd Edition)
2. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 2011 (6th Edition)
3. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002
4. Robert Sedgewick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
5. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", Willey, 2005

ECE18R5129 MEMORY TECHNOLOGIES AND TESTING

ECE18R5129 Memory Technologies and Testing	L	T	P	C
	3	0	0	3
Pre-requisite: ECE18R5104 VLSI Design Verification and Testing	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):

This course describes about the architectures of SRAM, DRAM and various non-volatile memories. Its addition to that it also describes fault modelling, testing of memories for fault detection, radiation hardening process and issues for memory

COURSE OUTCOME(S):

After completing this course, the student will be able to:

CO1: Understand types of memory and their usage
CO2: Compare different standard testing procedures for identifying memory fault
CO3: Demonstrate testability with fault tolerance
CO4: Analyse the factors like radiation and need for testing procedures
CO5: Understand and address the issues related to network functions and synthesis

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			M										L		
CO2	H	L													
CO3			M											L	
CO4	H		H	L							L		H		
CO5															L

COURSE TOPICS:

UNIT 1: RANDOM ACCESS MEMORY TECHNOLOGIES

Static Random-Access Memories (SRAMs), Dynamic Random-Access Memories (DRAMs). Overview, Masked Read-Only Memories (ROMs), Programmable Read-Only Memories (PROMs), Erasable (UV)-Programmable Read-Only Memories (EPROMs), Electrically Erasable PROMs (EEPROMs), Flash Memories (EPROMs or EEPROMs).

UNIT 2: MEMORY FAULT MODELLING AND TESTING

RAM Fault Modelling, RAM Electrical Testing, RAM Pseudorandom Testing, Megabit DRAM Testing, Non-volatile Memory modelling and Testing, IDDQ Fault modelling and Testing, Application Specific Memory Testing.

UNIT 3: MEMORY DFT AND FAULT TOLERANCE

General Design for Testability Techniques, RAM Built-in Self-Test (BIST), Embedded Memory DFT and BIST Techniques, Advanced BIST and Built-in Self-Repair Architectures, DFT and BIST for ROMs, Memory Error-Detection and Correction Techniques, Memory Fault-Tolerance Designs. General Reliability Issues, RAM Failure Modes and Mechanisms, Non-volatile Memory Reliability, Reliability modelling and Failure Rate Prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification.

UNIT 4: SEMICONDUCTOR MEMORY RADIATION EFFECTS

Radiation Effects, Radiation-Hardening Techniques, Radiation Hardness Assurance and Testing. Ferroelectric Random-Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto resistive Random-Access Memories (MRAMs), Experimental Memory Devices

UNIT 5: HIGH-DENSITY MEMORY PACKAGING TECHNOLOGIES

Memory Hybrids and MCMs (2-D), Memory Stacks and MCMs (3-D), Memory MCM Testing and Reliability Issues, Memory Cards, High-Density Memory Packaging Future Directions.

REFERENCE(S):

1. Ashok K. Sharma “Semiconductor Memories. Technology, Testing, and Reliability” Wiley 2013
2. Bernard Courtois, Thomas Wik, YervantZorian, “Memory Technology, Design and Testing”, IEEE / Wiley, 2008.

ECE18R5130SoC DESIGN

ECE18R5130SoC Design	Credits			
	L	T	P	Total
	3	0	0	3
Pre-requisite: Basics of Digital System Deign	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):

Give students an appreciation of the understanding of technological advances that allow us to integrate complete multi□processor systems on a single die, Systems□on-Chip(SoCs) are at

the coreofmostembeddedcomputingandconsumerdevices,suchas cell phones, media players andautomotive,aerospaceormedicalelectronics**.**

COURSE OUTCOME(S):

At the end of the course, students will be able to:

CO1: Identify and formulate a given problem in the framework of SoC based design approaches

CO2: Design SoC based system for engineering applications

CO3: Realize impact of SoC on electronic design philosophy and Macro-electronics thereby inclinetowards entrepreneurship andskill development.

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			M										L		
CO2	H	L													
CO3			M											L	

COURSE TOPICS:

UNIT 1: ASIC

Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP)concepts.

UNIT 2: NISC

NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction-set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modelling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.

UNIT 3: SIMULATION

Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modelling of data path design and control logic, Minimization of interconnects impact, clock tree design issues.

UNIT 4: LOW POWER SOC DESIGN / DIGITAL SYSTEM

Design synergy, Low power system perspective- power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimisation, building block memory, power down techniques, power consumption verification.

UNIT 5: SYNTHESIS

Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimisation constraints, Synthesis report analysis, Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs

Case study for overview of cellular phone design with emphasis on area optimisation, speed improvement and power minimization.

Note*:* Students will prepare and present a term paper on relevant identified current topics (in

batches of three students per topic) as a part of theory course.

REFERENCE(S):

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press 2008.
2. B. Al Hashimi, "System on Chip-Next generation Electronics", The IET 2006
3. RochitRajsuman, "System-on- a-chip: Design and Test", Advantest America R & D Centre, 2000
4. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann 2008
5. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley, 2011

ECE18R5131LOW POWER VLSI DESIGN

ECE18R5131Low Power VLSI Design	L	T	P	C
	3	0	0	3
Pre-requisite: ECE18R5103 Analog and Digital CMOS VLSI Design	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):

To expose the students to the low voltage device modelling, low voltage, low power VLSI CMOS circuit design.

COURSE OUTCOME(S):

At the end of the course, students will be able to:

CO1: Identify the sources of power dissipation in digital IC systems and understand the impact of power on system performance and reliability.

CO2: Characterize and model power consumption and understand the basic analysis methods.

CO3: Understand leakage sources and reduction techniques.

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			M										L		
CO2	H	L													
CO3			M											L	

COURSE TOPICS:

UNIT 1: TECHNOLOGY AND CIRCUIT DESIGN LEVELS

Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of VDD and Vt on speed, constraints on Vt reduction, transistor sizing and optimal gate oxide thickness, impact of technology scaling, technology innovations.

UNIT 2: LOW POWER CIRCUIT TECHNIQUES

Power consumption in circuits, flip-flops and latches, high capacitance nodes, energy

recovery, reversible pipelines, high performance approaches.

UNIT 3: LOW POWER CLOCK DISTRIBUTION

Power dissipation in clock distribution, single driver versus distributed buffers, buffersand device sizing under process variations, zero skew Vs. tolerable skew, chip and package co-design of clock network.

UNIT 4: LOGIC SYNTHESIS FOR LOW POWER ESTIMATION TECHNIQUES

Power minimization techniques, low power arithmetic components- circuit design styles, adders, multipliers.

UNIT 5: LOW POWER MEMORY DESIGN, LOW POWER MICROPROCESSOR DESIGN SYSTEM

Sources and reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM and SRAM, low power DRAM circuits, low power SRAM circuits.

Power management support, architectural trade-offs for power, choosing the supply voltage, low-power clocking, implementationproblemfor low power, comparison of microprocessors for power and performance.

REFERENCE(S):

1. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer 2002
2. Kaushik Roy, Sharat Prasad, "Low Power CMOS VLSI Circuit Design", Wiley 2000.
3. J.B. Kulo and J.H Lou, "Low Voltage CMOS VLSI Circuits", Wiley 1999.
4. A.P. ChandrasekaranandR.W. Broadersen,"LowPower DigitalCMOSdesign", Kluwer 1995
5. Gary Yeap, "Practical Low Power Digital VLSI Design", Kluwer 1998.

ECE18R5132COMMUNICATION BUSES AND INTERFACES

ECE18R5132 Communication Buses and Interfaces	L	T	P	C
	3	0	0	3
Pre-requisite: Basic Electronics	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):

To introduce various communication interfaces and their applications.
To introduce CAN and PCI protocols
To introduce developing of API for data transfer on serial bus
To teach students design and development of peripherals to do data transfer.

COURSE OUTCOME(S):

At the end of the course, students will be able to:
CO1: Select a serial bus suitable for anapplication.
CO2: Develop APIs for configuration, reading and writing data onto serial bus.
CO3: Design and develop peripherals that can be interfaced to desired serial bus.

Mapping of Course Outcome(s):

CO /	PO	PSO

PO	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			M										L		
CO2	H	L													
CO3			M											L	

COURSE TOPICS:

UNIT 1: SERIAL BUSSES

Physical interface, Data and Control signals, features.

UNIT 2: BUSES APPLICATIONS

Limitations and applications of RS232, RS 485, I^2C, SPI

UNIT 3:CAN

CAN: Architecture, Data transmission, Layers, Frame formats, applications

UNIT 4:PCIE

Revisions, Configuration space, Hardware protocols, applications

UNIT 5: USB, DATA STREAMING SERIAL COMMUNICATION PROTOCOL

Transfer types, enumeration, Descriptor types and contents, Device driver, Serial Front Panel Data Port (SFPDP) using fibre optic and copper cable

REFERENCE(S):

1. Jan Axelson, "Serial Port Complete - COM Ports, USB Virtual Com Ports, and Ports for Embedded Systems", Lakeview Research, 2ndEdition
2. Jan Axelson, "USB Complete", PenramPublications
3. Mike Jackson, Ravi Budruk, "PCI Express Technology", MindsharePress
4. Wilfried Voss, "A Comprehensible Guide to Controller Area Network", Copperhill Media Corporation, 2nd Edition,2005.
5. Serial Front Panel Draft Standard VITA 17.1 –200x
6. Technical references onwww.can-cia.org,www.pcisig.com,www.usb.org

ECE18R5135 PHYSICAL DESIGN AUTOMATION

ECE18R5135 Physical Design Automation	L	T	P	C
	3	0	0	3
Pre-requisite: ECE18R5102 Designing with ASICs	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):

The students will learn various design steps starting from system specifications to hardware/software implementation and will experience process optimisation while considering various design decisions in IC design.

COURSE OUTCOME(S):

At the end of the course, students will be able to:

CO1: Study automation process for VLSI System design.

CO2: Understanding of fundamentals for various physical design CAD tools.

CO3: Develop and enhance the existing algorithms and computational techniques for physical design process of VLSI systems.

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			L				M					L			
CO2						L									
CO3	L	L					H					L			

COURSE TOPICS:

UNIT 1:
Introduction to VLSI Physical Design Automation.

UNIT 2:
Standard cell, Performance issues in circuit layout, delay models Layout styles.

UNIT 3:
Discrete methods in global placement.

UNIT 4:
Timing-driven placement. Global Routing Via Minimization.

UNIT 5:
Over the Cell Routing - Single layer and two-layer routing, Clock and Power Routing. Compaction, algorithms, Physical Design Automation of FPGAs.

REFERENCE(S):

1. S. K. Lim, "Practical Problems in VLSI Physical Design Automation", Springer, 2008.
2. C. J. Alpert, D. P. Mehta, S. S. Sapatnekar, "Handbook of Algorithms for Physical Design Automation", Auerbach Publications, 2008
3. S. M. Sait and H. Youssef, "VLSI Physical Design Automation: Theory and Practice", World Scientific, 1999
4. T. H. Cormen, C. E. Leiserson, R. L. Rivest, C. Stein, "Introduction to Algorithms", MIT Press, 2009 (3rd edition)
5. Selected research papers from the literature.

ECE18R6120 HARDWARE SOFTWARE CO DESIGN

ECE18R6120Hardware Software Co-Design	L	T	P	C
	3	0	0	3
Pre-requisite: Basics of Digital System Design and Programming Basics	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):
The students will learn various design steps starting from system specifications to hardware/software implementation and will experience process optimisation while considering various design decisions.

COURSE OUTCOME(S):

After completing this course, the student will be able to:
CO1 Understand Serial and parallel communication protocols.
CO2 Model data flow and implement the same through software and hardware
CO3 Operate data flow using USB and CAN bus for PIC microcontrollers.
CO4 Design embedded Ethernet for Rabbit processors.
CO5 Design CORDIC and Crypto coprocessor

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			L				M					L			
CO2						L									
CO3	L	L					H					L			
CO4			M			L									
CO5		L					L								

COURSE TOPICS:

UNIT 1: THE NATURE OF HARDWARE AND SOFTWARE

Introducing Hardware/Software Co-design, The Quest for Energy Efficiency, The Driving Factors in Hardware/Software Co-design, The Dualism of Hardware Design and Software Design. Data Flow modelling and Transformation: Introducing Data Flow Graphs, Analysing Synchronous Data Flow Graphs, Control Flow modelling and the Limitations of Data Flow, Transformations.

UNIT 2: DATA FLOW IMPLEMENTATION

Software Implementation of Data Flow, Hardware Implementation of Data Flow, Hardware/Software Implementation of Data Flow

UNIT 3: ANALYSIS OF CONTROL FLOW AND DATA FLOW

Data and Control Edges of a C Program, Implementing Data and Control Edges, Construction of the Control Flow Graph Modern Bipolar, Transistor Structures, Construction of the Data Flow Graph.

UNIT 4: FINITE STATE MACHINE WITH DATAPATH

Cycle-Based Bit-Parallel Hardware, Hardware Modules, Finite State Machines with Data path, FSMD Design Example: A Median Processor

UNIT 5: SYSTEM ON CHIP

The System-on-Chip Concept, Four Design Principles in SoC Architecture, SoCModelling in GEZEL. Applications: Trivium Crypto-Coprocessor, CORDIC Co Processor.

REFERENCE(S):

1. Patrick R. Schaumont, “A Practical Introduction to Hardware/Software Co-Design”, Springer, 2013.
2. Jorgen Staunstrup, Wayne Wolf, “Hardware/Software Co-Design: Principles and Practice”, Kluwer, 2012.
3. Ralf Niemann, “Hardware/Software Co-Design for Data Flow Dominated Embedded Systems”, Kluwer, 1998.
4. Giovanni De Micheli, Rolf Ernst Morgon, “Reading in Hardware/Software Co-Design” Kaufmann, 2001.

ECE18R6121 THREE-DIMENSIONAL NETWORK-ON-CHIP

ECE18R6121Three-Dimensional Network-On-Chip	L	T	P	C
	3	0	0	3
Pre-requisite: SoC	**Course Category:** Program Specific Elective **Course type:** Theory			

COURSE OBJECTIVE(S):

NoC have been proposed as a promising solution for future SoC Design since it offers more scalability, allows more processors to operate concurrently and allows performance prediction. This course deals with overview to network on chip communication architecture, system integration, verification and testing of NOC in 3D

COURSE OUTCOME(S):

After completing this course, the student will be able to:

CO1: Understand different modelling and topologies of NoC

CO2: Describe the different communication architecture and integration in NoC

CO3: Address the challenges in Power and Thermal unit NoC testing and verification

CO4: Understand future of NoC in three dimensions

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	H										M		H		
CO2	H		H									H			
CO3	H			L						L	M				M
CO4	H		H						L					H	

COURSE TOPICS:

UNIT 1: INTRODUCTION TO NOC

SoC Integration and its Challenges, SoC to NoC: A Paradigm Shift, Research Issues in NoC Development, Existing NoC Examples, OSI Layer Roles in NoC, Benefits and Challenges in Adoption of NoCs, Topology Exploration, Traffic Modelling, Topology Modelling, Topology Synthesis, Application Mapping: Mapping Problem, ILP Formulation, Constructive Heuristics, Mapping using Discrete PSO

UNIT 2: NOC BASED SYSTEM INTEGRATION

Switching Technique, Packet Routing, QoS, Congestion Control and Flow Control, Router Design, Network Link Design, NoC Interface Design, Clock Distribution, NoC Based System Floor Planning

UNIT 3: NOC VERIFICATION AND TESTING

Models, Wear-out Mechanisms, Faults Classification, Fault Tolerance Metrics, Error Control Coding for On-Chip signalling, Power and Energy Savings in NoCs, On Designing Reliable NoCs, NoC Verification, Testing Fundamentals, NoC Testing

UNIT 4: NOC DESIGN AND PROTOTYPING FRAMEWORK

The Spidergon ST NoC, Middleware Memory Management in NoC, The Sysmantic Framework, Application Specific NoC Synthesis, Reconfigurable NoC Design

UNIT 5: DESIGN OF 3-D NOCS

3-D Integration, Design and Evaluation of 3-D NoC Architectures, Case Studies: Implementation of a 3-D Instance for LEON3 Processor, Implementation of a 3-D NoC, Future Trends: Photonic NoC, Wireless NoCs

REFERENCE(S):

1. KonstantinosTatas, Kostas Siozios, DimitriosSoudris, Axel Jantsch, "Designing 2D and 3D Network-on-Chip Architectures", Springer, 2014.
2. Aida Todri-Sanial, ChauanSeng Tan, "Physical design for 3D Integrated Circuits", CRC Press, 2015.
3. SantanuKundu, SantanuChattopadhyay, "Network-on-Chip: The Next Generation of System-on-Chip Integration", CRC Press, 2014.
4. Abbas Sheibanyrad, FrédéricPétrot, Axel Jantsch, "3D Integration for NoC-based SoC Architectures", Springer, 2010.

ECE18R6122 QUANTUM ELECTRONICS

ECE18R6122Quantum Electronics	L	T	P	C
	3	0	0	3
Pre-requisite: BasicPhysics	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):

This course describes about various types of transistors, lasers and general concepts of photon detectors. In addition to that it also describes super lattice, quantum dot photo diodes and tera Hz devices

COURSE OUTCOME(S):

After completing this course, the student will be able to:

CO1: Understand the semiconductor junction types and operations
CO2: Describe the principles of operation, development and usage of lasers
CO3: Understand the Electro thermal properties and classification of photo diodes
CO4: Compare the different material for photo detector manufacturing and characterization
CO5: Analyse the new technology in devices and technology related to photo diode

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1	H														
CO2	H	L	M										H		
CO3	H					M					L				
CO4		L													L
CO5	H		H			L			L			H		H	

COURSE TOPICS:

UNIT 1: SEMICONDUCTORS AND TRANSISTORS

Overview, Ideal *p-n* junction at equilibrium, Non-equilibrium properties of *p-n* junctions. Metal-semiconductor junctions, Overview of amplification and switching, bipolar junction transistors, Hetero junction bipolar transistors, Field effect transistors, Application specific transistors.

UNIT 2: LASERS

Overview, Types of lasers, General laser theory, Ruby laser, Semiconductor lasers, Basic operation principles, the components of a quantum cascade laser, Making a quantum cascade laser, Device performance, Wall plug efficiency optimisation, Power scaling, Photonic crystal distributed feedback quantum cascade lasers, Quantum cascade lasers at different wavelengths.

UNIT 3: PHOTO DETECTORS

Overview, Electromagnetic radiation, Photo detector parameters, Thermal detectors, Types of photon detectors, Examples of photon detectors, Focal Plane Arrays, Overview, Avalanche photo detectors, linear mode, Examples of APD structures, Geiger mode operation

UNIT 4: QUANTUM DOT INFRARED PHOTO DETECTORS

Overview, Material system and variants of Type II superlattices, Physics of Type II InAs/GaSb Superlattices, Advantages of Type II superlattice, Material growth and characterization, Device fabrication. Advantages of QDIPs, Quantum dot fabrication for QDIPs, Review of actual QDIP performance.

UNIT 5: TERA-HERTZ DEVICE TECHNOLOGY

Single-photon avalanche photodiodes, Broadband terahertz sources, Narrow band terahertz sources, Quantum cascade terahertz sources, Magnetic field effects, Difference frequency generation, GaN QCLs for high temperature operation.

REFERENCE(S):

1.ManijehRazeghi, “Technology of Quantam device”, Springer, 2010.
2. Benjamin Fain, “Quantum electronics”, Pergamon Press, 1969.

ECE18R6123 NANOMATERIALS AND NANOTECHNOLOGY

ECE18R6123 Nanomaterials and Nanotechnology	L	T	P	C
	3	0	0	3
Pre-requisite: Basic Physics	**Course Category:** Program Specific Elective **Course Type:** Theory			

COURSE OBJECTIVE(S):

To learn the basic science behind the fabrication of nanomaterials.

To study the new solutions for current problems and competing technologies for future applications.

To study the inter disciplinary projects applicable to wide areas

To study the operation of fabrication and characterisation devices to achieve precisely designed systems

COURSE OUTCOME(S):

At the end of the course, students will be able to:

CO1: To understand the basic science behind the design and fabrication of Nano scale systems.
CO2: To understand and formulate new engineering solutions for current problems and competing technologies for future applications.
CO3: To be able make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.
CO4: To gather detailed knowledge of the operation of fabrication and characterisation devices to achieve precisely designed systems.

Mapping of Course Outcome(s):

CO / PO	PO												PSO		
	1	2	3	4	5	6	7	8	9	10	11	12	1	2	3
CO1			L												L
CO2	H	L							M		L		H		
CO3	H											H		H	
CO4	H	L	H						M						

COURSE TOPICS:

UNIT 1:
Nanomaterials in one and higher dimensions,

UNIT 2:
Applications of one and higher dimension Nanomaterials.

UNIT 3:
Nanolithography, micro electro-mechanical system (MEMS) and Nano-phonics.

UNIT 4:
Carbon nanotubes – synthesis and applications

UNIT 5:
Interdisciplinary arena of nanotechnology.

REFERENCE(S):

1. Kenneth J. Kaunda and Ryan M. Richards (Editors), “Nanoscale Materials in Chemistry”, Wiley,2009 (2nd edition).
2. A I Gusev and A ARempel, “Nanocrystalline Materials”, Cambridge Publishing, 2008.
3. Bharat Bhushan, “Springer Handbook of Nanotechnology” Springer, 2010 (3rd edition).
4. Kamal K. Kar, “Carbon Nanotubes: Synthesis, Characterization and Applications”, Research Publishing Services, 2011.

ECE18R5141 BASICS OF VLSI DESIGN

ECE18R5141 Basics of VLSI Design	L	T	P	C
	3	0	0	3
Pre-requisite: --	**Course Type:** Interdisciplinary Elective **Course Category:** Theory			

COURSE OBJECTIVE:

The main objectives of this course are, make the students to understand

The VLSI design flow and manufacturing process, Basic characteristics of MOS transistor and examine various possibilities for configuring inverter circuits and aspects of latch-up, Design processes aided by simple concepts such as stick and symbolic diagrams with set of design rules and scaling factors, Basic circuit concepts and parameters for MOS processes which greatly ease the design process, How the Integrated Circuits are implemented in different ways

COURSE OUTCOME(S):

CO1: Explain the chip fabrication technology.
CO2: Explain the characteristics of CMOS transistors
CO3: Explain the layout rules and scaling effects in VLSI circuit design
CO4: Identify the interactions between process parameters device structures, circuit performance and system design
CO5: Explain the various ways of implementing Integrated Circuits

COURSE TOPICS:

UNIT 1: VLSI DESIGN FLOW AND FABRICATION

VLSI Design flow: History of VLSI, VLSI Circuit Design Process, Design flow, Design strategies

VLSI Fabrication: Process technologies, Process steps in MOSFET fabrication, Wafer manufacture, Wafer cleaning, Doping and impurities, Growth and deposition, Masking and lithography, Etching, Metallisation and interconnects, Packaging (encapsulation), Fabrication of passive components

UNIT 2: ELECTRICAL PROPERTIES OF MOS

nMOS, pMOS Transistor, Enhancement and depletion transistor, Leakage current in MOSFET, AC properties of MOSFET, nMOS Inverter, CMOS Logic, Pass transistor and transmission logic, Pull up to Pull down ratio (Driven by another nMOS inverter, Driven by one or more pass transistor), Alternative forms of pull-up, CMOS Inverter, MOS Device design equations, Ideal I-V Characteristics, C-V Characteristics, Latch-up in CMOS circuits

UNIT 3: VLSI CIRCUIT DESIGN PROCESS

Basic CMOS technology, MOS layers, Stick Diagrams, Layout, Design rules, Double metal MOS process rules, CMOS Lambda based rules, layer assignments.

CMOS Scaling: Scaling models and scaling factors, Scaling parameters, Difficulties arising due to scaling

UNIT 4: CIRCUIT CONCEPTS

Sheet resistance, Sheet resistance concept applied to MOS capacitors and inverters, Area capacitance of layers, Standard unit of capacitance, The Delay Unit, Inverter delays, Driving large capacitive loads, Propagation delays

UNIT 5:SEMICONDUCTOR IC DESIGN

Implementation approaches in VLSI Design, Programmable Logic Devices, Programmable Logic Arrays, Programmable Array Logic, Field Programmable Gate Arrays, Standard Cells, Design issues, Requirements of a successful chip design, Power consumption, Reliability, Need for testing, Challenges in VLSI Design

REFERENCE(S):

1. K. Lal Kishore, V.S.V. Prabhakar, "VLSI Design", I. K. International Pvt Ltd, 2009
2. Douglas A. Pucknell, Kamran Eshraghian, "Basic VLSI Design", PHI, 2008 (3rd Edition)
3. Partha Pratim Sahu, VLSI Design, McGraw Hill, 2013.
4. Neil H. E. Weste, David Harris, CMOS VLSI Design, Pearson India, 4th Edition, 2011

ECE18R5142 CMOS IC DESIGN

ECE18R5142 CMOS IC Design	L	T	P	C
	3	0	0	3
Pre-requisite: --	**Course Type:** Interdisciplinary Elective **Course Category:** Theory			

COURSE OBJECTIVE:

The objective is to make students acquire the knowledge of MOS Transistor, learn the design of CMOS Logic circuits and subsystems

COURSE OUTCOME(S):

CO1: Explain the design flow and styles of VLSI Circuits
CO2: Explain the characteristics of MOS and its design rules
CO3: Demonstrate an understanding of design of digital circuits using CMOS
CO4: Demonstrate an understanding of design of analog circuits using CMOS
CO5: Demonstrate an understanding of design of mixed signal circuits using CMOS

COURSE TOPICS:

UNIT 1: VLSI DESIGN BASICS

Evolution – Application – Quality metrics – VLSI Design flow – Physical Design Cycle – Design styles – CMOS Logic

UNIT 2: CMOS PROPERTIES AND CIRCUIT DESIGN

Characteristics – Second order effects – Scaling – Design process of MOSFET based devices – Design rules – Stick Diagram – Mask Layout

UNIT 3: CMOS BASED DIGITAL DESIGN

CMOS Inverter - CMOS NAND Gate – CMOS NOR Gate – Combinational Digital Circuit – Sequential Digital Circuit – Transmission Gate - Memory

UNIT 4: CMOS BASED ANALOG DESIGN

Passive Components – Current Source/Sink – Voltage Dividers – Amplifiers – Operational Amplifier

UNIT 5: CMOS MIXED SIGNAL DESIGN

Adaptive Biasing – CMOS Comparator – Analog Multipliers – Level Shifting – Dynamic Mixed Signal Circuit – Data Converters

REFERENCE(S):

1. Partha Pratim Sahu, "VLSI Design", McGraw Hill, 2013
2. Vikrant Vij, Nidhi Syal, "VLSI Design Theory and Practice", University Science Press (Laxmi Publications), 2013
3. Neil H. E. Weste, David Harris, "CMOS VLSI Design", Pearson, 4th Edition, 2011
4. Kiran Kumar V.G. and Nagesh H.R., "Fundamentals of VLSI Design", Pearson, 2011

ECE18R6141 DIGITAL DESIGN USING VERILOG HDL

ECE18R6141 Digital Design using Verilog HDL	L	T	P	C
	3	0	0	3
Pre-requisite: --	**Course Type:** Interdisciplinary Elective **Course Category:** Theory			

COURSE OBJECTIVE:

At the end of the course the student will be able to analyse, design and implementation of digital circuits using synthesisable HDL.

COURSE OUTCOME(S):

CO1: Demonstrate knowledge on Verilog HDL
CO2: Apply knowledge of HDL to design combinational circuits.
CO3: Apply knowledge of HDL to design sequential circuits
CO4: Apply knowledge of Verilog HDL to design complex digital system

COURSE TOPICS:

UNIT 1: VERILOG HDL BASICS

VLSI Design Flow and Methodologies, Verilog Design description, Verilog operators

UNIT 2: COMBINATIONAL CIRCUIT DESIGN

Logic gates and synthesisable RTL, Arithmetic Circuits, Multiplexer, Decoders, Encoders

UNIT 3: COMBINATIONAL CIRCUIT DESIGN GUIDELINES

Use of blocking assignments and event queue, Incomplete sensitivity list, Continuous versus Procedural assignments, Combinational loops in design, Unintentional latches in design, If-Else versus Case statement, Missing 'default' clause in Case statement, If-Else with Else missing, Logical equality versus Case equality, Arithmetic Resource sharing, Multiple driver assignment

UNIT 4: SEQUENTIAL CIRCUIT DESIGN

Sequential logic, Flip-flop, Synchronous and Asynchronous reset, Synchronous counters, Asynchronous counters, Memory modules and design, Blocking and non-blocking

assignments use, Synchronous versus asynchronous reset use, Internally Generated Clocks, Gated Clocks, Use of pipelining in design, Guidelines for modelling synchronous and asynchronous designs, Multiple clocks and multi-phase clocks

UNIT 5: COMPLEX DESIGNS

Functions and tasks, ALU Design, Parity generators and detectors, Barrel shifters

REFERENCE(S):

1. Vaibbhav Taraate, "Digital Logic Design Using Verilog: Coding and RTL Synthesis", Springer, 2016
2. Charles Roth, Lizy Kurian John and Byeong Kil Lee, "Digital Systems Design Using Verilog", Cengage, 2016
3. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson, 2015 (2nd Edition 2003 Reprint)
4. Donald Leach, Albert Malvino, Goutam Saha, Digital Principles and Applications, McGraw Hill, 8th Edition (SIE), 2014